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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,992	01/31/2002	Steven Teig	SPLX.P0096	2859

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EXAMINER	
LU, KUEN S	

ART UNIT	PAPER NUMBER
2167	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,992	TEIG ET AL.	
	Examiner	Art Unit	
	Kuen S. Lu	2167	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendments

1. The Action is responsive to Applicant's Amendments, filed on November 15, 2005. The Amendments made to amend claims 1, 3-4, 9, 11, 13-14 and 19 is noted.

2. Please note new issue was raised when the amended element "the data storage structure stores each sub-network ~~based on~~ **indexed by** a parameter derived from all ~~the~~ output functions of the sub-network", specifically the high-lighted, was introduced to each of the independent claims 1 and 11. The new issue would require further consideration and/or new search. Please see MPEP 706.07(b).

3. Concerning Applicant's Remarks on claim rejections, filed on November 15, 2005 has been fully considered by the Examiner. Please see discussion in the section ***Response to Arguments***, following the Action, as shown next.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1 and 3-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Pedersen et al. (U. S. Patent 6,134,705, hereafter "Pedersen"), in view of Ho et al. (U.S. Patent 6,009,251, hereafter "Ho").

As per claim 1, concerning "A data storage structure that stores a plurality of sub-networks," at col. 12, lines 4-9 Pedersen teaches comparing old and new un-synthesized sub-netlists which suggests the sub-netlists data structures are stored and retrieved, and Pedersen further teaches "wherein each sub-network performs" functions at col. 14, lines 17-40 and Figs. 7A-7F, nodes u and v, where sub-netlists perform output functions.

Pedersen does not explicitly teach data storage structure to store sub-network and each network performs at least three output functions, although Pedersen does suggest sub-netlists data structures are stored and retrieved as described above.

However, Ho teaches integrated circuit design and sub-designs are retrieved and stored in database and files at Fig. 4A and col. 11, lines 39-41 and col. 1, lines 61-64, and a sub-network performs multiple, at least three, output functions at Figs. 2B and 4B, and col. 14, lines 37-40 where an integrated circuit cell consists of three sub-cells each having its output ports for performing output functions.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention was made to combine Ho's teaching with Pedersen reference by applying the integrated circuit multiple cells and sub-cells verification to identify a multiple number of logic cells because both references are directed to verifying or

identifying the electronic circuit design, and the combined teaching of the two references would have provided a method for both efficiently and correctly verifying and identifying the design of integrated circuit having multiple number of components.

The combined teaching of the Ho and Pedersen references further teaches "wherein the data storage stores each sub-network indexed by a parameter derived from all output functions of the sub-network" (See Ho: col. 7, lines 11-111-14 and 27-36 where cell contains specific references to sub-cell design, including information on geometry, connectivity and inter-connections information, further, each parent sub-cell design that references other child sub-cell designs also contains information regarding the manner in which the child sub-cells are connected together and/or connected to any local structure of the parent sub-cell).

As per claim 11, concerning "A data storage structure that stores a plurality of sub-networks," at col. 12, lines 4-9 Pedersen teaches comparing old and new un-synthesized sub-netlists which suggests the sub-netlists data structures are stored and retrieved, and Pedersen further teaches "wherein each sub-network performs" functions at col. 14, lines 17-40 and Figs. 7A-7F, nodes u and v, where sub-netlists perform output functions.

Pedersen does not explicitly teach data storage structure to store sub-network and each network performs at least three output functions, although Pedersen does suggest sub-netlists data structures are stored and retrieved as described above.

However, Ho teaches integrated circuit design and sub-designs are retrieved and stored in database and files at Fig. 4A and col. 11, lines 39-41 and col. 1, lines 61-64, and a sub-network performs multiple, at least three, output functions at Figs. 2B and 4B, and col. 14, lines 37-40 where an integrated circuit cell consists of three sub-cells each having its output ports for performing output functions.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention was made to combine Ho's teaching with Pedersen reference by applying the integrated circuit multiple cells and sub-cells verification to identify a multiple number of logic cells because both references are directed to verifying or identifying the electronic circuit design, and the combined teaching of the two references would have provided a method for both efficiently and correctly verifying and identifying the design of integrated circuit having multiple number of components.

The combined teaching of the Ho and Pedersen references further teaches the following:

"wherein the data storage stores each sub-network indexed by a parameter derived from all output functions of the sub-network" (See Ho: col. 7, lines 11-111-14 and 27-36 where cell contains specific references to sub-cell design, including information on geometry, connectivity and inter-connections information, further, each parent sub-cell design that references other child sub-cell designs also contains information regarding the manner in which the child sub-cells are connected together and/or connected to any local structure of the parent sub-cell); and

"a data access manager that identifies and retrieves sub-networks from the data storage structure" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled).

As per claim 3, the combined teaching of the Ho and Pedersen references further teaches the following:

"each sub-network includes a set of circuit elements" (See Pedersen: Fig. 7A and col. 14, lines 17-32 where the netlist consists of gates, clock and registers);

"the data storage structure stores each sub-network in terms of (i) an encoding of a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network" (See Pedersen: at col. 6, lines 20-23 where electronic design is provided as a high level Boolean representation, encoded in a hardware design language and as schematic or any other form representing the logical arrangement of a device, and at col. 1, lines 37-43 referencing U.S. Patent Application 08/958,778 where Southgate states a fully described block diagram stored in a graphic design file at col. 4, lines 65-67); and

"(ii) a set of local functions that includes a local function for each node of the graph" (See Pedersen: Fig. 7E where a set of local functions include the functions at nodes u and v).

As per claim 4, the combined teaching of the Ho and Pedersen references further teaches "the data storage structure stores, for each sub-network, an identifier that specifies the set of local functions and the graph" (See Pedersen: col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware).

As per claim 5, the combined teaching of the Ho and Pedersen references further teaches "the identifier for each sub-network specifies the locations that store the set of local functions and the graph of the particular sub-network" (See Pedersen: Figs. 4A-4B and at col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware).

As per claims 6 and 16, the combined teaching of the Ho and Pedersen references further teaches "the identifier for each sub-network is a set of indices that specifies the set of local functions and the graph of the sub-network" (See Pedersen: Figs. 4A-4B and col. 11, lines 62-66, col. 12, lines 10-15 and 43-45, and col. 13, lines 28-38 and 43-54 where an identified sub-netlist is analyzed for its gates locations and nodes functions).

As per claims 7 and 17, the combined teaching of the Ho and Pedersen references further teaches "the set of indices for each sub-network includes a graph index and a set of function indices, wherein, for each sub-network, the graph index identifies the

storage location of the graph for the sub-network, and each function index identifies the storage location of a local function of the sub-network" (See Pedersen Figs. 4A-4B and col. 6, lines 29-35 and 54-59 where gates and nodes are selected from the synthesize and un-synthesized sub-netlist one by one for analysis).

As per claims 8 and 18, the combined teaching of the Ho and Pedersen references further teaches "the storage structure is a database, and the graphs are stored in a graph table, the local functions are stored in at least one function table, wherein each graph index specifies a record in the graph table, and each function index specifies a record in the function table" (See Pedersen: Fig. 7A and col. 1, lines 37-44 and Southgate: at col. 9, lines 28-36 and 41-49 where graphic editor uses graphic design database for reading from writing to the graphic design block diagram for integrated circuit and interacts with hierarchy information database which stores the hierarchy information files for each IC design).

As per claims 9 and 19, the combined teaching of the Ho and Pedersen references further teaches "the local functions are stored in multiple function tables, wherein a first function table is for n-input functions, and a second function table is for m-input functions, where n and m are integers, wherein some of the function indices specify functions in the first function table while other function indices specify functions in the second function table" (See Pedersen: Fig. 7D where sub-netlists 762, 764 and 766 each has two inputs and one output functions while 776 has four and two, respectively).

As per claim 10, the combined teaching of the Ho and Pedersen references further teaches "the data storage structure associates the generated parameter for each sub-network with the graph and function identifier for the sub-network" (See Pedersen: col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware).

As per claim 12, the combined teaching of the Ho and Pedersen references further teaches "the data access manager receives a parameter, the manager searches the data storage structure for sub-networks that are stored based on the received parameter, and if the manager finds a sub-network that is stored based on the received parameter, the manager retrieves the sub-network" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 43-50 where user input the changed design for receiving and retrieving the sub-netlist to be incrementally recompiled).

As per claim 13, the combined teaching of the Ho and Pedersen references further teaches the following:
"each sub-network includes a set of circuit elements" (See Pedersen: Fig. 7A and col. 14, lines 17-32 where the netlist consists of gates, clock and registers);
"the data storage structure stores each sub-network in terms of (i) an encoding of a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network" (See

Pedersen: at col. 6, lines 20-23 where electronic design is provided as a high level Boolean representation, encoded in a hardware design language and as schematic or any other form representing the logical arrangement of a device, and at col. 1, lines 37-43 referencing U.S. Patent Application 08/958,778 where Southgate states a fully described block diagram stored in a graphic design file at col. 4, lines 65-67); and

"(ii) a set of local functions that includes a local function for each node of the graph" (See Pedersen: Fig. 7E where a set of local functions include the functions at nodes u and v) ; and

"for each retrieved sub-network, the manager retrieves the graph and the set of local functions of the sub-network" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled).

As per claim 14, the combined teaching of the Ho and Pedersen references further teaches the following:

"the data storage structure stores, for each sub-network, an identifier that specifies the set of local functions and the graph" (See Pedersen: col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware);

"the data storage structure associates the generated parameter for each sub-network with the graph and function identifier for each sub-network" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where the compiler conducts a the process for

identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled); and

"the manager uses the received parameter to identify an identifier associated with the received parameter, and then uses the identified identifier to retrieve a graph and a set of local functions" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where user is allowed to input changed design for identifying the new gates such the incremental synthesized process can start).

As per claim 15, the combined teaching of the Ho and Pedersen references further teaches "the manager uses the received parameter to identify a set of identifiers associated with the received parameter, and then use the identified set of identifiers to retrieve graphs and sets of local functions that specify several sub-network" (See Pedersen: Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled).

6. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Pedersen et al. (U. S. Patent 6,134,705, hereafter "Pedersen") in view of Ho et al. (U.S. Patent 6,009,251, hereafter "Ho") as applied to claims 1 and 3-19 above, and further in view of Moreaux (U.S. Patent 6,925,088).

As per claims 20 and 21, the combined teaching of Pedersen and Ho teaches "each sub-network comprises a set of circuit elements" (See Pedersen: Figs. 7A-7D where sub-netlist comprises a set of circuit elements).

The combined teaching of Pedersen and Ho references does not explicitly teach "at least some of the sub-networks comprise a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit".

However, Moreaux teaches "at least some of the sub-networks comprise a first circuit having a first output outside the sub-network and a second circuit having a second output outside the sub-network, wherein the first circuit receives a direct or indirect input from the second circuit" at Fig. 3 wherein a subnet connects star distributors (elements 301s) and peripheral units or devices (elements 302s). Note the three elements 302s at the most right side in the Figure, as a first circuits, receives direct or indirect input from the two elements 301, the second circuits. Also note the elements 302s and 301s are all outside of the central subnet, the element 320 at the center in the Figure.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention was made to combine the teaching of Moreaux with Ho and Pedersen references for further enhance the flexibility of circuit design such that a more compact of electronic design is possible for flexibly selecting electronic components and decrementing the need of more special hardware.

Conclusions

7. The prior art made of record

A. U. S. Patent No. 6,134,705

G. U. S. Patent No. 6,925,088

H. U. S. Patent No. 6,009,251

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

B. U. S. Patent No. 6,110,223

C. U. S. Patent No. 6,102,964

D. U. S. Patent No. 5,201,046

E. U. S. Patent No. 5,440,720

F. U. S. Patent No. 6,272,529

I. U. S. Patent No. 5,956,257

Response to Arguments

8. The Applicants' arguments filed on November 11, 2005, have been fully considered. As for the Examiner's response, please see discussion below.

a). At Pages 7 and 10, concerning claims 1 and 11, Applicant argued that Pedersen does not teach data storage for storing sub-networks.

As to the above argument **a)**, Examiner respectfully submits that, by comparing old and new un-synthesized sub-netlists at col. 12, lines 4-9, Pedersen does suggest the teaching of sub-netlists data structures being stored and retrieved. Examiner further submits that the explicit teaching of data storage for storing sub-networks does come from Ho reference by showing that integrated circuit design and sub-designs are

retrieved and stored in database and files at Fig. 4A and col. 11, lines 39-41 and col. 1, lines 61-64,

b). At Pages 8 and 10, concerning claims 1 and 11, Applicant argued that Pedersen does not disclose a method of indexing a data structure.

As to the above argument **b)**, Examiner respectfully submits that the newly introduced Ho reference provides the teaching. Please refer to the earlier Office Action for details.

c). At Pages 8 and 11, concerning claims 1 and 11, Applicant argued that neither Pedersen nor Lum reference discloses a network performing three output function.

As to the above argument **c)**, Examiner respectfully submits that the newly introduced Ho reference provides the teaching. Please refer to the earlier Office Action for details.

Conclusions

9. Applicant's amendment necessitated the new grounds of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Kuen S. Lu whose telephone number is (571) 272-4114. The examiner can normally be reached on Monday-Friday (8:30 am - 5:30 pm). If attempts to reach the examiner by telephone pre unsuccessful, the Examiner's Supervisor, Jean R. Homere, Esq. can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for Page 13 Published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact he Electronic Business Center (EBC) at 886-217-9197 (toll-free).

Kuen S. Lu
Patent Examiner

February 5, 2006